MINISTRY OF SCIENCE AND TECHNOLOGY

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PROJECT REPORT

ON

AUTOMATIC WATER TANK FILLING CIRCUIT

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ABSTRACT

Automatic water tank filling circuit is constructed by using step-down transformers, full wave bridge rectifier. CD 4011 quad2 input NAND Gate IC, C945 transistor and 12V relay. It consists of power supply circuit, latch, transistor as a switch circuit and relay driver circuit. If this circuit is used, we do not need to switch on or off water pump motor and water level in the tank is down from the limited. On the other hand, if the water reached to the high level, the water pump motor is automatically switched off. So, this circuit is used to prevent the water pump motor from the short life of motor and reaching in meter units consumed.

CHAPTER 1

INTRODUCTION

Every apartment of the cities and other towns use the tanks. The water pump is switch on when we cannot see the water level in the tank. We remember that switch off when water fills over the tank. Usually, the pump is switch on, for the fitting water in the tank that does not know how much water is. In the same way, we remember pump switch off, when we hear water flow down over the tank. So it is not only the raising in meter units consumed but also is the short life of pump when pump do not need to switch on. For preventing the above cases, we use this circuit.

There are two basic forms of control system:

(a) Open loop system

(b) Closed loop system

In our project, we use closed loop system for automatic water tank filling circuit.

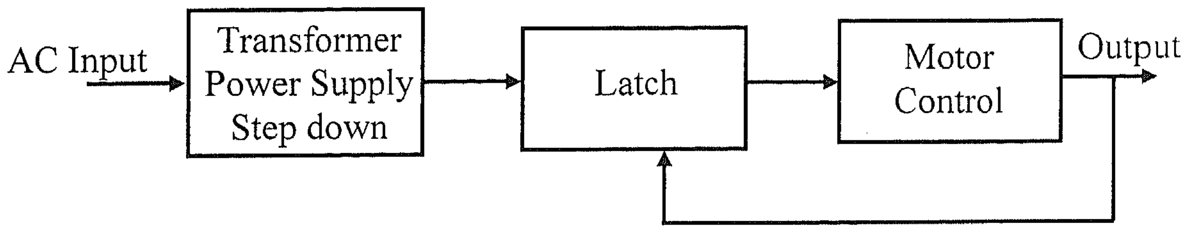


Figure (1.1) Block Diagram of the Automatic Water Tank Filling Circuit

CHAPTER 2

POWER SUPPLY

2.1 Full-Wave Bridge Rectifier

When the input cycle is positive, diodes D_1 and D_2 are forward-biased and conduct current through R_L. During this time, diodes D_3 and D_4 are reverse-biased.

When the input cycle is negative as shown in Figure, diodes D_3 and D_4 are forward-biased and conduct current in the same direction through R_L as during the positive half-cycle. During the negative half-cycle, D_1 and D_2 are reversed-biased.

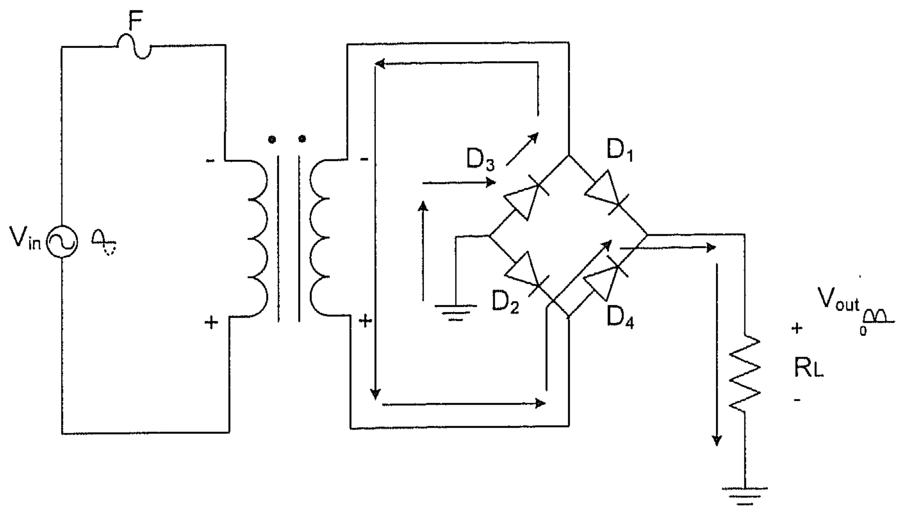


Fig: Full Wave Bridge Rectifier

(1) Peak value of output:

$$V_{P(out)} = V_{P(\sec)} - 1.4V$$

(2) Average value of output:

$$V_{AVG} = \frac{2V_{P(out)}}{\pi}$$

(3) Diode peak inverse voltage:

$$PIV = V_{P(out)} + 0.7\text{ V}$$

Type Number	PIV	$I_{F(max)}$
IN 4001	50 V	1 A
IN 4002	100 V	1 A
IN 4003	200 V	1 A
IN 4004	400 V	1 A
IN 4005	600 V	1 A
IN 4006	800 V	1 A
IN 4007	1000 V	1 A

Electrical Characteristics of 1A Diodes

Type Number	PIV	$I_{F(max)}$
IN 5400	50 V	3 A
IN 5401	100 V	3 A
IN 5402	200 V	3 A
IN 5403	300 V	3 A
IN 5404	400 V	3 A
IN 5405	500 V	3 A
IN 5406	600 V	3 A
IN 5407	700 V	3 A
IN 5408	800 V	3 A

Electrical Characteristics of 3A Diodes

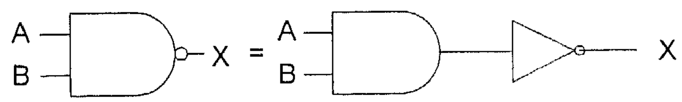
CHAPTER 3

LATCHES

The Latch is a type of bi-stable storage device that is normally placed in a category separate from that of flip-flops. Latches are basically similar to flip-flops because they are bi-stable device that can reside in either of two states by virtue of a feedback arrangement, in which the outputs are connected back to the opposite input.

3.1 The NAND GATE

The NAND gate is a popular logic element because it can be used as a universal gate: that is NAND gates can be used in combination to perform the AND, OR and inverter operations.



Distinctive shape, 2 input NAND gate and its NOT/AND equivalent

In a 2 input NAND gate operation, output x is LOW if inputs A and B are HIGH: X is HIGH if either A or B is LOW, or if both A and B are LOW.

Input		**Output**
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

1 = HIGH, 0 = LOW

Truth Table for a 2 input NAND gate

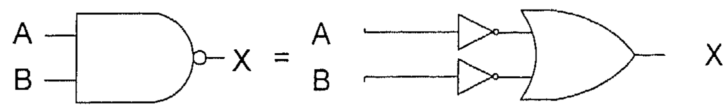
In practical terms, De Morgan's theorems provide mathematical verification of the equivalency of the NAND and negative OR gate.

De Morgan's First Theorem is stated as:

The complement of a product of variables is equal to the sum of the complement of the variables.

Stated another way

The complement of two or more variables ANDed is equivalent to the OR of the complements of the individual variables.



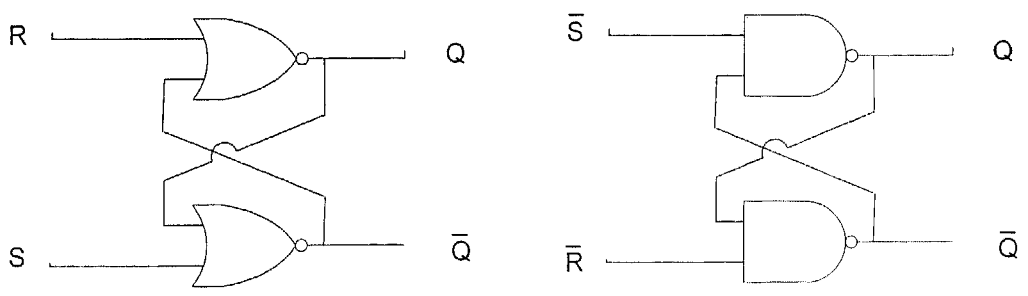
NAND Negative OR

A	B	$\overline{AB}$	$\overline{A} + \overline{B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

3.2 The S.R Latch

3.2.1 The Basic Structure of S.R Latch

A latch is a type of bistable mulivibrator. An active HIGH input S.R (SET RESET) latch is formed with two-cross-coupled NOR gates. An active LOW input $\overline{S}.\overline{R}$ latch is formed with two-cross-coupled NAND gates. The output of each gate is connected to an input of the opposite gate. This produces the regenerative feedback that is characteristics of multivibrators.



(a) Active-HIGH input S.R Latch (b) Active-LOW input $\overline{S}.\overline{R}$ Latch

Two versions of SET-RESET (S.R) Latches

3.2.2 The Operation of S.R Latch

To understand the operation of the Latch, we will use the NAND gates $\overline{S}.\overline{R}$ latch. This latch is redrawn with the negative OR equivalents used for the NAND gates. This is done because LOWs on the $\overline{S}$ and $\overline{R}$ lines are the activating inputs. The latch has two inputs $\overline{S}$ and $\overline{R}$, and two outputs, Q and $\overline{Q}$. Lets start by assuming that both input and the Q output are HIGH. Since the Q output is connected back to an input of gate G_2 must be LOW. This LOW output is coupled back to an input of gate G_1, ensuring that its output is HIGH.

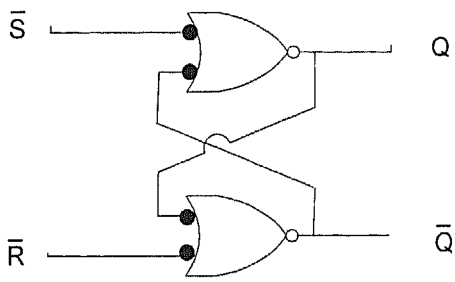


Fig: Negative-OR equivalent of the NAND gate $\overline{S}.\overline{R}$ Latch

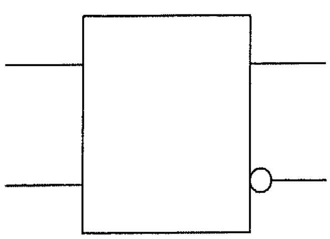
When the Q output is HIGH, the latch is in the SET State. It will remain in this state indefinitely until a low is temporarily applied to the $\overline{R}$ input. With a LOW on the $\overline{R}$ input and a HIGH on $\overline{S}$, the output of gate G_2 is forced HIGH. This HIGH on the $\overline{Q}$ output is coupled the back to input of G_1 and since the S input is HIGH, the output of G_1 goes LOW. This LOW on the Q output is then coupled back to an input of G_2 ensuring that Q output remains HIGH even when the LOW on the $\overline{R}$ input is removed. When the Q output is LOW, the latch is in the RESET State. Now the latch remains indefinitely in the RESET state until a LOW is applied to the $\overline{S}$ input.

The outputs of the latch are always complements of each other. When Q is HIGH, $\overline{Q}$ is LOW, and when Q is LOW, $\overline{Q}$ is HIGH. An a valid conditions, in the operation of an active LOW inputs $\overline{S}$-$\overline{R}$ latch occurs when LOW are applied to both $\overline{S}$ and $\overline{R}$at the same time. As long as the LOW simultaneously held on the inputs, both Q and $\overline{Q}$ outputs are forced HIGH, thus violating the basic complementary operations of the output. Also if the LOWs are released simultaneously, both outputs will attempt to go LOW. Since there is always some small different in the propagation delay time of the gates, one of the gates will dominate in its transition to the LOW output state. This, in turn, forces the output of the slower gate to remain HIGH. In this saturation, you cannot reliably predict the next state of the latch.

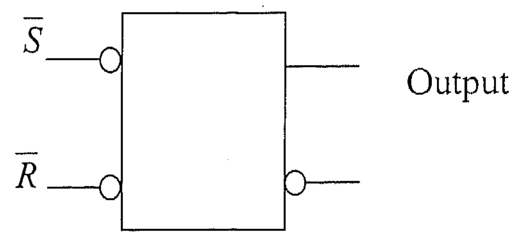
The active LOW input $\overline{S}$-$\overline{R}$ latch operation for each of the four possible combinations of levels on the inputs. Table summarizes the logical operation in truth table form. Operation of the active HIGH input NOR gate latch is similar but requires the use of the opposite logic levels.

Inputs		Outputs		Comments
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
1	1	NC	NC	No Change latch remains present state
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
0	0	1	1	Invalid condition

Truth Table for an Active-LOW input $\overline{S}$ - $\overline{R}$ latch condition



(a) Active-HIGH input S.R Latch



(b) Active-LOW input $\overline{S}$ - $\overline{R}$ latch

Logic symbols for S.R Latch

Logic symbols for both the active-HIGH input and the active-LOW input latches.

How on active-LOW input $\overline{S}$ - $\overline{R}$ latch responds to condition on its inputs. LOW levels are pulsed on each input in a certain sequence and the resulting Q output waveform is observed. The $\overline{S}$ = 0, $\overline{R}$ = 0 condition is avoided because it results in an invalid mode of operation and is a major of any SET-RESET type of latch.

CHAPTER 4

MOTOR CONTROL

4.1 The Operation of Transistor as a Switch

When input voltage is supplied,

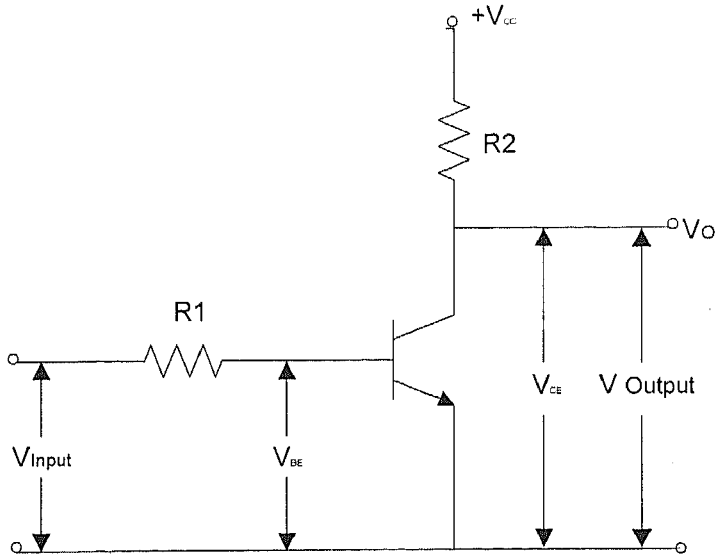


Fig: Transistor ON State.

R_1 is chosen to obtain maximum base current, if V_{BE} is greater and equal to 0.7V. So transistor is saturation state. V_{CE} is 0V and collector current is calculated by $\frac{V_{CC}}{R_2}$. When input voltage is shorted,

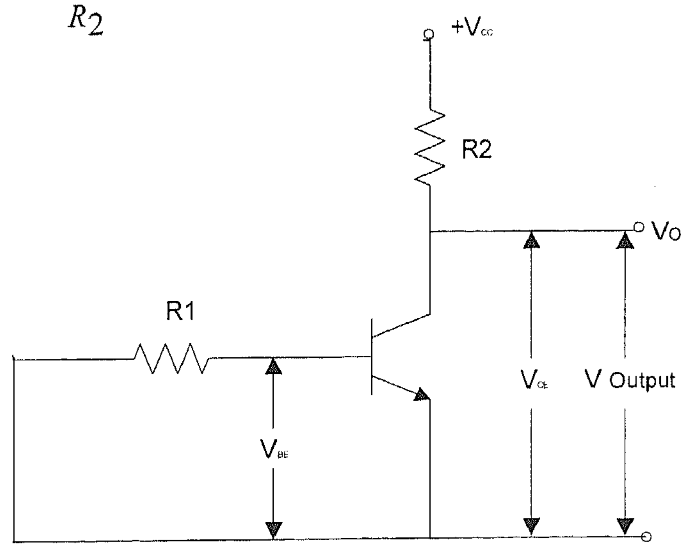


Fig: Transistor OFF State

V_{BE} is less than 0.7V and collector current does not flow. V_{CE} is equal to V_{CC}, and the transistor is cutoff state.

Type Number	Type	h_{FE}	V_{CEO} volt	$I_{c\,max}$ mA	F_T MHz	P_D mW
2SC828	npn	65-700	30	50	220	250
2SC828A	npn	65-700	45	50	220	250
2SC829	npn	65-700	30	30	230	250
2SC945	npn	200	60	100	250	250

Table * Electronic Characteristic of npn transistors*

4.2 Electromagnetic Relay

Electromagnetic relay is used for controlling AC volt by automatic transformer and safe-guard. It is automatically control to reduce voltage, to rise voltage and to cutoff voltage whenever AC main voltage is over or down from the limiting voltage.

(a) (b)

Relay Symbols

4.2.1 Operation of relay

At shown in figure, in the relay coil does not flow the current while switch S_1 turn on. This in time, armature is contact to the upward due to attracting of spring. When middle terminal C is contact terminal NC, L_1 will light. When switch S_1 turn off, soft-iron core become magnetize and draw to the downward armature. Since relay coil is flowed by the current. Middle terminal is contact C away from the NC and contact to the NO. Therefore L_1 is off and L_2 is on. If the control current can made automatically cutting, it would connected many power consuming electronic and electronic device giving to electrical power.